

CLAIMS

What is claimed:

- 1 1. A system for clearing data residing in a memory region, comprising:
 2 a controller; and
 3 a memory coupled to said controller having said memory region subdivided into a
 4 plurality of sub-regions, each said sub-region comprising a plurality of storage elements
 5 wherein said controller is designed to write clear data concurrently to each one of said
 6 plurality of sub-regions.
- 1 2. The system of claim 1, wherein said memory region is subdivided into
 2 four sub-regions.
- 1 3. The system of claim 1, wherein said memory region is subdivided into
 2 consecutive and adjacent sub-regions.
- 1 4. The system of claim 1, wherein said memory region is subdivided into
 2 sub-regions that are of equal dimension.
- 1 5. The system of claim 1, wherein said memory region is subdivided into
 2 sub-regions that vary in dimension.
- 1 6. The system of claim 1, wherein said clear data corresponds to a predefined
 2 color of a pixel.
- 1 7. The system of claim 1, wherein said memory is a frame buffer associated
 2 with a graphics display device.
- 1 8. The system of claim 1, wherein said controller is a frame buffer controller.

1 9. The system of claim 1, wherein said plurality of sub-regions are
2 individually identified by location in said memory by a pointer register.

1 10. The system of claim 1, further comprising a processor configured to
2 determine the location of said memory region.

1 11. The system of claim 10, wherein said processor transmits a single clear
2 command to said controller, wherein said controller is prompted to clear each one of said
3 plurality of sub-regions.

1 12. The system of claim 10, wherein said processor transmits a plurality of
2 clear commands to said controller, wherein each one of said clear commands corresponds
3 to one of each said plurality of sub-regions.

1 13. The system of claim 10, wherein said processor determines the location of
2 said memory region based upon a dimension and a position of an at least one image to be
3 written to a graphics display device.

1 14. The system of claim 10, wherein said processor determines the location of
2 a plurality of memory regions based upon a dimension and a position of a plurality of
3 images, such that one of each said plurality of memory regions corresponds to one of said
4 plurality of views.

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1 17. The method of claim 15, further comprising the step of issuing a plurality
2 of clear commands, wherein each one of said clear commands corresponds to one of each
3 said plurality of sub-regions, and wherein the step of issuing said plurality of clear
4 commands initiates said step of writing.

1 18. The method of claim 15, further comprising the step of associating a
2 plurality of location identifiers, wherein one location identifier is associated with each
3 one of said plurality of sub-regions residing in said frame buffer, and wherein said step of
4 concurrently writing clear data begins at said plurality of sub-regions identified by said
5 plurality of corresponding location identifiers.

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1 20. A computer readable medium having a program for clearing data residing
2 in a memory region, the program comprising logic configured to perform the steps of:
3 determining a dimension and a position of at least one image displayed on a video
4 display device, wherein said at least one image is to be cleared;
5 determining a location of said memory region where a plurality of data having at
6 least pixel information associated with a plurality of pixels which display said at least one
7 image is stored;
8 subdividing said memory region into a plurality of sub-regions; and
9 writing said clear data concurrently to each of said plurality of sub-regions.

1 21. A system for clearing data residing in a memory region, comprising:
2 means for determining a dimension and a position of at least one image displayed
3 on said graphics display device, wherein said at least one image is to be cleared;
4 means for determining a location of a region of memory where a plurality of data
5 having at least pixel information associated with a plurality of pixels which display said
6 at least one image is stored;
7 means for subdividing said memory region into a plurality of sub-regions; and
8 means for writing said clear data concurrently to each of said plurality of sub-
9 regions.

1 22. The system of claim 21, further comprising means for associating a
2 plurality of location identifiers, wherein one location identifier is associated with each
3 one of said plurality of sub-regions residing in said frame buffer, and wherein said means
4 for concurrently writing clear data begins at said plurality of sub-regions identified by
5 said plurality of corresponding location identifiers.

- 1 23. The system of claim 22, further comprising means for determining said
2 dimension and said position for each one of a plurality of images, and wherein said
3 means of determining a location and said means for subdividing said memory region
4 operates on each one of said plurality of images.

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